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10/625,617	07/24/2003	Tokuroh Ozawa	100629.03	7916

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EXAMINER	
LESPERANCE, JEAN E	

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,617	OZAWA ET AL.	
	Examiner	Art Unit	
	Jean E. Lesperance	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/24/2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/24/03, 10-24-03, 11-6-03, 6-10-04* 2-9-05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 to 14 are presented for examination.

2. The Information Disclosure Statements filed July 24, 2003, October 24, 2003, November 6, 2003, June 10, 2004 and February 9, 2005 are considered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over 5,670,792 (Utsugi et al.).

Regarding claim 1, Utsugi et al. teach a plurality of scanning lines Fig.2 (103); a plurality of data lines (101); a plurality of common power supply lines Fig.2 (106); and a plurality of pixels Fig.2 (130), each pixel of the plurality of pixels comprising: a first transistor Fig.2 (Qs) having a first gate electrode that is connected to a respective scanning line of the plurality of scanning lines (103); a second transistor (QI) to control conduction between a respective common power supply line (106) of the plurality of common power supply lines (106); and a luminescent element Fig.2 (EL) provided between a pixel electrode and an opposite electrode opposed to the pixel electrode, the

capacitor C then has its terminal voltage applied between a gate and a source of the current-controlling transistor Q.sub.I so that, depending on a drain current vs. gate voltage characteristic of the transistor Q.sub.I a current is conducted from the power supply electrode line 105 through the luminescent element EL and the transistor Q.sub.I to a common electrode line 106, making the luminescent element EL luminesce. It therefore is possible to make the luminescent element EL luminesce with a preset luminance determined from a relationship between the luminance of the element EL and the imposed voltage on the capacitor C. Moreover, the applied voltage between the gate and the source of the current-controlling transistor Q.sub.I is maintained by a quantity of stored charges in the capacitor C, at a substantially constant voltage for a predetermined time period (column 3, lines 10-25) corresponding to the potential the respective common power supply line being higher than a potential of the opposite electrode when the each pixel is "on", and the potential of the pixel electrode being higher than the potential of the opposite electrode when the each pixel is "on". The prior art does not explicitly teaches the potential the respective common power supply line being higher than a potential of the opposite electrode when the each pixel is "on", and the potential of the pixel electrode being higher than the potential of the opposite electrode when the each pixel is "on". However, the prior art teaches the capacitor C then has its terminal voltage applied between a gate and a source of the current-controlling transistor Q.sub.I so that, depending on a drain current vs. gate voltage characteristic of the transistor Q.sub.I a current is conducted from the power supply electrode line 105 through the luminescent element EL and the transistor Q.sub.I to a

common electrode line 106, making the luminescent element EL luminesce. It therefore is possible to make the luminescent element EL luminesce with a preset luminance determined from a relationship between the luminance of the element EL and the imposed voltage on the capacitor C. Moreover, the applied voltage between the gate and the source of the current-controlling transistor Q.sub.I is maintained by a quantity of stored charges in the capacitor C, at a substantially constant voltage for a predetermined time period (column 3, lines 10-25). It would have been obvious to a person of ordinary skill in the art to modify teaches the capacitor C then has its terminal voltage applied between a gate and a source of the current-controlling transistor Q.sub.I so that, depending on a drain current vs. gate voltage characteristic of the transistor Q.sub.I a current is conducted from the power supply electrode line 105 through the luminescent element EL and the transistor Q.sub.I to a common electrode line 106, making the luminescent element EL luminesce. It therefore is possible to make the luminescent element EL luminesce with a preset luminance determined from a relationship between the luminance of the element EL and the imposed voltage on the capacitor C. Moreover, the applied voltage between the gate and the source of the current-controlling transistor Q.sub.I is maintained by a quantity of stored charges in the capacitor C, at a substantially constant voltage for a predetermined time period (column 3, lines 10-25) to achieve the potential the respective common power supply line being higher than a potential of the opposite electrode when the each pixel is "on", and the potential of the pixel electrode being higher than the potential of the opposite electrode

when the each pixel is "on" because this would provide a current controlled luminous element array of high quality active matrix type.

Regarding claim 2, Regarding claim 1, Utsugi et al. teach a plurality of scanning lines Fig.2 (103); a plurality of data lines (101); a plurality of common power supply lines Fig.2 (106); and a plurality of pixels Fig.2 (130), each pixel of the plurality of pixels comprising: a first transistor Fig.2 (Qs) having a first gate electrode that is connected to a respective scanning line of the plurality of scanning lines (103); a second transistor (QI) to control conduction between a respective common power supply line (106) of the plurality of common power supply lines (106); and a luminescent element Fig.2 (EL) provided between a pixel electrode and an opposite electrode opposed to the pixel electrode, the capacitor C then has its terminal voltage applied between a gate and a source of the current-controlling transistor Q.sub.I so that, depending on a drain current vs. gate voltage characteristic of the transistor Q.sub.I a current is conducted from the power supply electrode line 105 through the luminescent element EL and the transistor Q.sub.I to a common electrode line 106, making the luminescent element EL luminesce. It therefore is possible to make the luminescent element EL luminesce with a preset luminance determined from a relationship between the luminance of the element EL and the imposed voltage on the capacitor C. Moreover, the applied voltage between the gate and the source of the current-controlling transistor Q.sub.I is maintained by a quantity of stored charges in the capacitor C, at a substantially constant voltage for a predetermined time period (column 3, lines 10-25) corresponding to the potential of the respective common power supply line being higher than the potential of the opposite

electrode when a current flows from the respective power supply line to the opposite electrode, and the potential of the pixel electrode being higher than the potential of the opposite electrode when a current flows from the respective power supply line to the opposite electrode.

Regarding claim 3, Utsugi et al. teach a plurality of scanning lines Fig.2 (103); a plurality of data lines (101); a plurality of common power supply lines Fig.2 (106); and a plurality of pixels Fig.2 (130), each pixel of the plurality of pixels comprising: a first transistor Fig.2 (Qs) having a first gate electrode that is connected to a respective scanning line of the plurality of scanning lines (103); a second transistor (QI) to control conduction between a respective common power supply line (106) of the plurality of common power supply lines (106); and a luminescent element Fig.2 (EL) provided between a pixel electrode and an opposite electrode opposed to the pixel electrode, the capacitor C then has its terminal voltage applied between a gate and a source of the current-controlling transistor Q.sub.I so that, depending on a drain current vs. gate voltage characteristic of the transistor Q.sub.I a current is conducted from the power supply electrode line 105 through the luminescent element EL and the transistor Q.sub.I to a common electrode line 106, making the luminescent element EL luminesce. It therefore is possible to make the luminescent element EL luminesce with a preset luminance determined from a relationship between the luminance of the element EL and the imposed voltage on the capacitor C. Moreover, the applied voltage between the gate and the source of the current-controlling transistor Q.sub.I is maintained by a quantity of stored charges in the capacitor C, at a substantially constant voltage for a

predetermined time period (column 3, lines 10-25) corresponding to the potential of the respective common power supply line being higher than the potential of the opposite electrode when a current flows from the respective power supply line to the opposite electrode, the potential of the pixel electrode being higher than the potential of the opposite electrode and a lower than the potential of the respective common power supply line when a current flows from the respective power supply line to the opposite electrode.

Regarding claim 4, Utsugi et al. teach a plurality of scanning lines Fig.2 (103); a plurality of data lines (101); a plurality of common power supply lines Fig.2 (106); and a plurality of pixels Fig.2 (130), each pixel of the plurality of pixels comprising: a first transistor Fig.2 (Qs) having a first gate electrode that is connected to a respective scanning line of the plurality of scanning lines (103); a second transistor (QI) to control conduction between a respective common power supply line (106) of the plurality of common power supply lines (106); and a luminescent element Fig.2 (EL) provided between a pixel electrode and an opposite electrode opposed to the pixel electrode, the capacitor C then has its terminal voltage applied between a gate and a source of the current-controlling transistor Q.sub.I so that, depending on a drain current vs. gate voltage characteristic of the transistor Q.sub.I a current is conducted from the power supply electrode line 105 through the luminescent element EL and the transistor Q.sub.I to a common electrode line 106, making the luminescent element EL luminesce. It therefore is possible to make the luminescent element EL luminesce with a preset luminance determined from a relationship between the luminance of the element EL and

the imposed voltage on the capacitor C. Moreover, the applied voltage between the gate and the source of the current-controlling transistor Q.sub.I is maintained by a quantity of stored charges in the capacitor C, at a substantially constant voltage for a predetermined time period (column 3, lines 10-25) corresponding to the potential of the respective common power supply line being higher than the potential of the opposite electrode when the driving current flows from the respective power supply line to the opposite electrode, and the potential of the pixel electrode being higher than the potential of the opposite electrode when the driving current flows from the respective power supply line to the opposite electrode.

Regarding claim 5, Utsugi et al. teach a plurality of scanning lines Fig.2 (103); a plurality of common power supply lines Fig.2 (106); and a plurality of pixels Fig.2 (130), each pixel of the plurality of pixels comprising: a first transistor Fig.2 (Qs) having a first gate electrode that is connected to a respective scanning line of the plurality of scanning lines (103); a second transistor (QI) to control conduction between a respective common power supply line (106) of the plurality of common power supply lines (106); and a luminescent element Fig.2 (EL) provided between a pixel electrode and an opposite electrode opposed to the pixel electrode, the luminescent element being able to emit a light due to a driving current that flows from the pixel electrode to the opposite electrode, the capacitor C then has its terminal voltage applied between a gate and a source of the current-controlling transistor Q.sub.I so that, depending on a drain current vs. gate voltage characteristic of the transistor Q.sub.I a current is conducted from the power supply electrode line 105 through the luminescent element EL and the transistor

Q.sub.I to a common electrode line 106, making the luminescent element EL luminesce. It therefore is possible to make the luminescent element EL luminesce with a preset luminance determined from a relationship between the luminance of the element EL and the imposed voltage on the capacitor C. Moreover, the applied voltage between the gate and the source of the current-controlling transistor Q.sub.I is maintained by a quantity of stored charges in the capacitor C, at a substantially constant voltage for a predetermined time period (column 3, lines 10-25) corresponding to the potential of the second gate electrode being lower than or being equal to the potential of the respective common power supply line, and the potential of the respective common power supply line being higher than the potential of the opposite electrode when a current flows from the respective power supply line to the opposite electrode.

Regarding claim 6, Utsugi et al. teach a plurality of scanning lines Fig.2 (103); a plurality of common power supply lines Fig.2 (106); and a plurality of pixels Fig.2 (130), each pixel of the plurality of pixels comprising: a first transistor Fig.2 (Qs) having a first gate electrode that is connected to a respective scanning line of the plurality of scanning lines (103); a second transistor (QI) to control conduction between a respective common power supply line (106) of the plurality of common power supply lines (106); and a luminescent element Fig.2 (EL) provided between a pixel electrode and an opposite electrode opposed to the pixel electrode, the luminescent element being able to emit a light due to a driving current that flows from the pixel electrode to the opposite electrode, the capacitor C then has its terminal voltage applied between a gate and a source of the current-controlling transistor Q.sub.I so that, depending on a drain current

vs. gate voltage characteristic of the transistor Q.sub.I a current is conducted from the power supply electrode line 105 through the luminescent element EL and the transistor Q.sub.I to a common electrode line 106, making the luminescent element EL luminesce. It therefore is possible to make the luminescent element EL luminesce with a preset luminance determined from a relationship between the luminance of the element EL and the imposed voltage on the capacitor C. Moreover, the applied voltage between the gate and the source of the current-controlling transistor Q.sub.I is maintained by a quantity of stored charges in the capacitor C, at a substantially constant voltage for a predetermined time period (column 3, lines 10-25) corresponding to the potential of the second gate electrode being higher than or being equal to the potential of the opposite electrode, and the potential of the respective common power supply line being higher than the potential of the opposite electrode when a current flows from the respective power supply line to the opposite electrode.

Regarding claim 7, Utsugi et al. teach a plurality of scanning lines Fig.2 (103); a plurality of data lines (101); a plurality of common power supply lines Fig.2 (106); and a plurality of pixels Fig.2 (130), each pixel of the plurality of pixels comprising: a first transistor Fig.2 (Qs) having a first gate electrode that is connected to a respective scanning line of the plurality of scanning lines (103); a second transistor (QI) to control conduction between a respective common power supply line (106) of the plurality of common power supply lines (106); and a luminescent element Fig.2 (EL) provided between a pixel electrode and an opposite electrode opposed to the pixel electrode, the luminescent element being able to emit a light due to a driving current that flows from

the pixel electrode to the opposite electrode, the capacitor C then has its terminal voltage applied between a gate and a source of the current-controlling transistor Q.sub.I so that, depending on a drain current vs. gate voltage characteristic of the transistor Q.sub.I a current is conducted from the power supply electrode line 105 through the luminescent element EL and the transistor Q.sub.I to a common electrode line 106, making the luminescent element EL luminesce. It therefore is possible to make the luminescent element EL luminesce with a preset luminance determined from a relationship between the luminance of the element EL and the imposed voltage on the capacitor C. Moreover, the applied voltage between the gate and the source of the current-controlling transistor Q.sub.I is maintained by a quantity of stored charges in the capacitor C, at a substantially constant voltage for a predetermined time period (column 3, lines 10-25) corresponding to the potential of the second gate electrode being higher than or being equal to the potential of the opposite electrode, and the potential of the respective common power supply line being higher than the potential of the opposite electrode when a current flows from the respective power supply line to the opposite electrode.

Regarding claim 8, Utsugi et al. teach a current-controlling transistor Q.sub.I in a picture element 10 in one row has a source electrode thereof, i.e. an electrode thereof at the opposite end to another connected to a luminescent element EL, connected to a scan electrode line 3.sub.N. in an adjacent previous row, and a charge holding capacitor C in the same picture element 10 has one electrode thereof, i.e. one of two electrodes thereof at the opposite end to the other connected to a gate electrode of the

transistor Q.sub.I, connected to the same scan electrode line 3.sub.N (column 5, lines 63-67) and (column 6, lines 1-5) corresponding to the first transistor and the second transistor being of opposite conduction type each other.

Regarding claim 9, Utsugi et al. teach a plurality of scanning lines Fig.2 (103); a plurality of data lines (101); a plurality of common power supply lines Fig.2 (106); and a plurality of pixels Fig.2 (130), each pixel of the plurality of pixels comprising: a first transistor Fig.2 (Qs) having a first gate electrode that is connected to a respective scanning line of the plurality of scanning lines (103); a second transistor (QI) to control conduction between a respective common power supply line (106) of the plurality of common power supply lines (106); and a luminescent element Fig.2 (EL) provided between a pixel electrode and an opposite electrode opposed to the pixel electrode, the luminescent element being able to emit a light due to a driving current that flows from the pixel electrode to the opposite electrode, the capacitor C then has its terminal voltage applied between a gate and a source of the current-controlling transistor Q.sub.I so that, depending on a drain current vs. gate voltage characteristic of the transistor Q.sub.I a current is conducted from the power supply electrode line 105 through the luminescent element EL and the transistor Q.sub.I to a common electrode line 106, making the luminescent element EL luminesce. It therefore is possible to make the luminescent element EL luminesce with a preset luminance determined from a relationship between the luminance of the element EL and the imposed voltage on the capacitor C. Moreover, the applied voltage between the gate and the source of the current-controlling transistor Q.sub.I is maintained by a quantity of stored charges in the

capacitor C, at a substantially constant voltage for a predetermined time period (column 3, lines 10-25) corresponding to the potential of the respective common power supply line being higher than the potential of the opposite electrode when a current flows from the respective power supply line to the opposite electrode and the switching transistor Q.sub.S then turns off, and the charge holding capacitor C holds there across the imposed voltage from the signal electrode line 1.sub.M. The capacitor C thus has its terminal voltage applied between the gate and source electrodes of the current-controlling transistor Q.sub.I so that, according to a drain current vs. gate voltage characteristic of the transistor Q.sub.I, an electric current runs through an established conducting route: the power source electrode line 5.fwdarw.the luminescent element EL.fwdarw.the transistor Q.sub.I .fwdarw.the scan electrode line causing the luminescent element EL to luminesce (column 8, lines 18-28) corresponding to the potential of a data signal to turn off the each pixel being lower than or being equal to the potential of the respective common power supply line.

Regarding claim 10, Utsugi et al. teach the second transistor (QI) being of P-channel type.

Regarding claim 11, Utsugi et al. teach the second transistor (Qs) being of P-channel type.

Regarding claim 12, Utsugi et al. teach a plurality of scanning lines Fig.2 (103); a plurality of data lines (101); a plurality of common power supply lines Fig.2 (106); and a plurality of pixels Fig.2 (130), each pixel of the plurality of pixels comprising: a first transistor Fig.2 (Qs) having a first gate electrode that is connected to a respective

scanning line of the plurality of scanning lines (103); a second transistor (QI) to control conduction between a respective common power supply line (106) of the plurality of common power supply lines (106); and a luminescent element Fig.2 (EL) provided between a pixel electrode and an opposite electrode opposed to the pixel electrode, the capacitor C then has its terminal voltage applied between a gate and a source of the current-controlling transistor Q.sub.I so that, depending on a drain current vs. gate voltage characteristic of the transistor Q.sub.I a current is conducted from the power supply electrode line 105 through the luminescent element EL and the transistor Q.sub.I to a common electrode line 106, making the luminescent element EL luminesce. It therefore is possible to make the luminescent element EL luminesce with a preset luminance determined from a relationship between the luminance of the element EL and the imposed voltage on the capacitor C. Moreover, the applied voltage between the gate and the source of the current-controlling transistor Q.sub.I is maintained by a quantity of stored charges in the capacitor C, at a substantially constant voltage for a predetermined time period (column 3, lines 10-25) corresponding to the potential of the pixel electrode being higher than the potential of the opposite electrode.

Regarding claim 13, Utsugi et al. teach a plurality of scanning lines Fig.2 (103); a plurality of data lines (101); a plurality of common power supply lines Fig.2 (106); and a plurality of pixels Fig.2 (130), each pixel of the plurality of pixels comprising: a first transistor Fig.2 (Qs) having a first gate electrode that is connected to a respective scanning line of the plurality of scanning lines (103); a second transistor (QI) to control conduction between a respective common power supply line (106) of the plurality of

common power supply lines (106); and a luminescent element Fig.2 (EL) being able to emit a light due to a driving current that flows from the pixel electrode to the opposite electrode, the potential of a data signal to turn on the each pixel being higher than or being equal to the potential of the opposite electrode provided between a pixel electrode and an opposite electrode opposed to the pixel electrode, the capacitor C then has its terminal voltage applied between a gate and a source of the current-controlling transistor Q.sub.I so that, depending on a drain current vs. gate voltage characteristic of the transistor Q.sub.I a current is conducted from the power supply electrode line 105 through the luminescent element EL and the transistor Q.sub.I to a common electrode line 106, making the luminescent element EL luminesce. It therefore is possible to make the luminescent element EL luminesce with a preset luminance determined from a relationship between the luminance of the element EL and the imposed voltage on the capacitor C. Moreover, the applied voltage between the gate and the source of the current-controlling transistor Q.sub.I is maintained by a quantity of stored charges in the capacitor C, at a substantially constant voltage for a predetermined time period (column 3, lines 10-25) corresponding to the potential of a data signal to turn on the each pixel being higher than or being equal to the potential of the opposite electrode, and the potential of the respective common power supply line being higher than the potential of the opposite electrode when a current flows from the respective power supply line to the opposite electrode.

Regarding claim 14, Utsugi et al. teach the second transistor (Qs) being of P-channel type.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (571) 272-7692. The examiner can normally be reached on from Monday to Friday between 10:OOAM and 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard, can be reached on (571) 272-7603.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance

Art Unit 2674

Date 6/9/2005

HENRY N. TRAN
PRIMARY EXAMINER